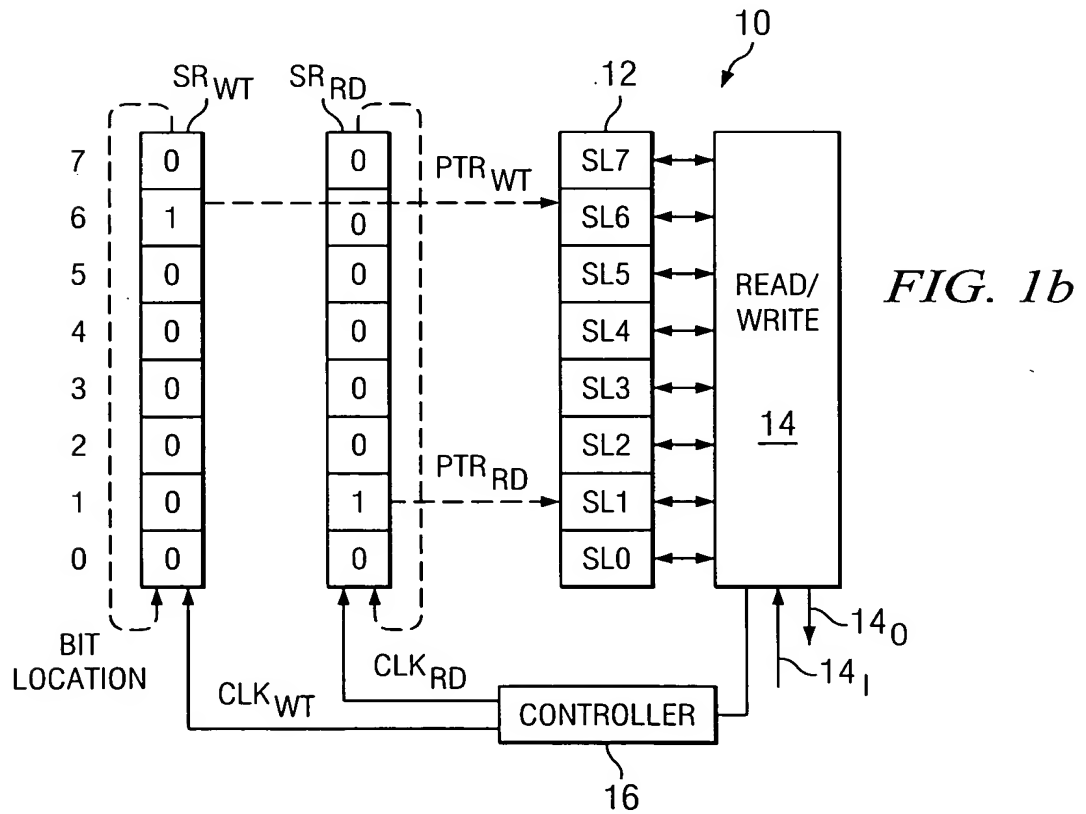
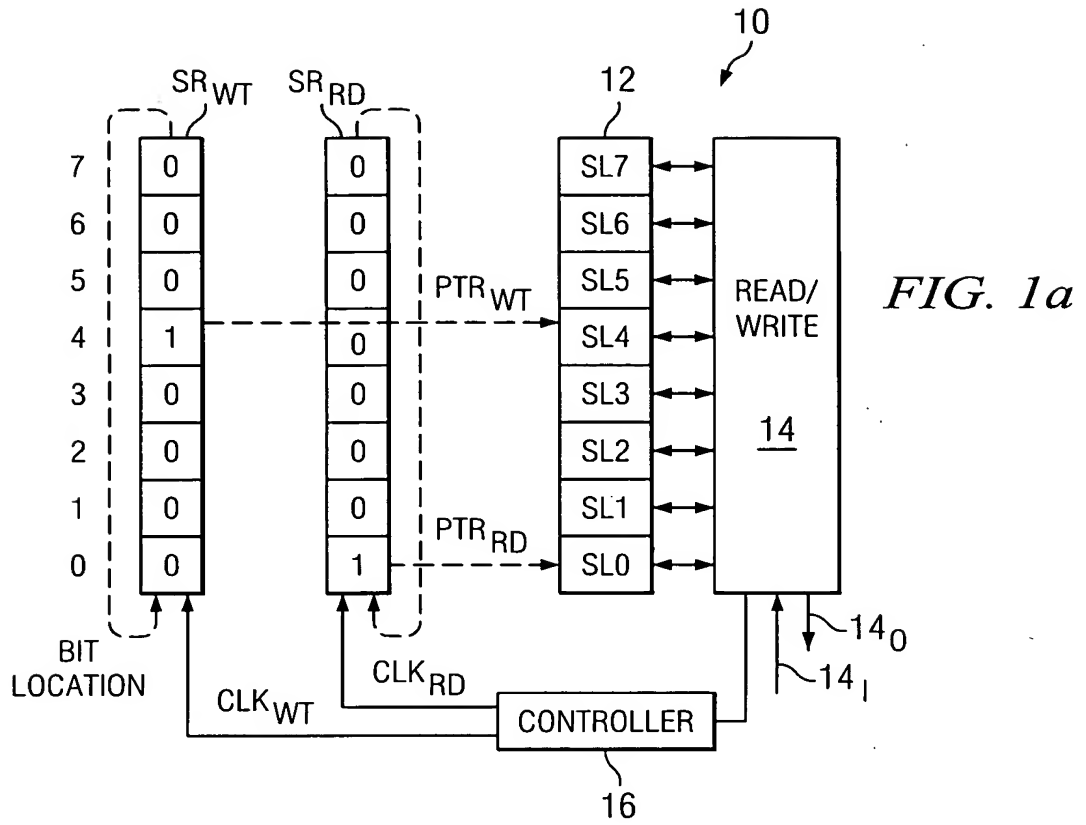
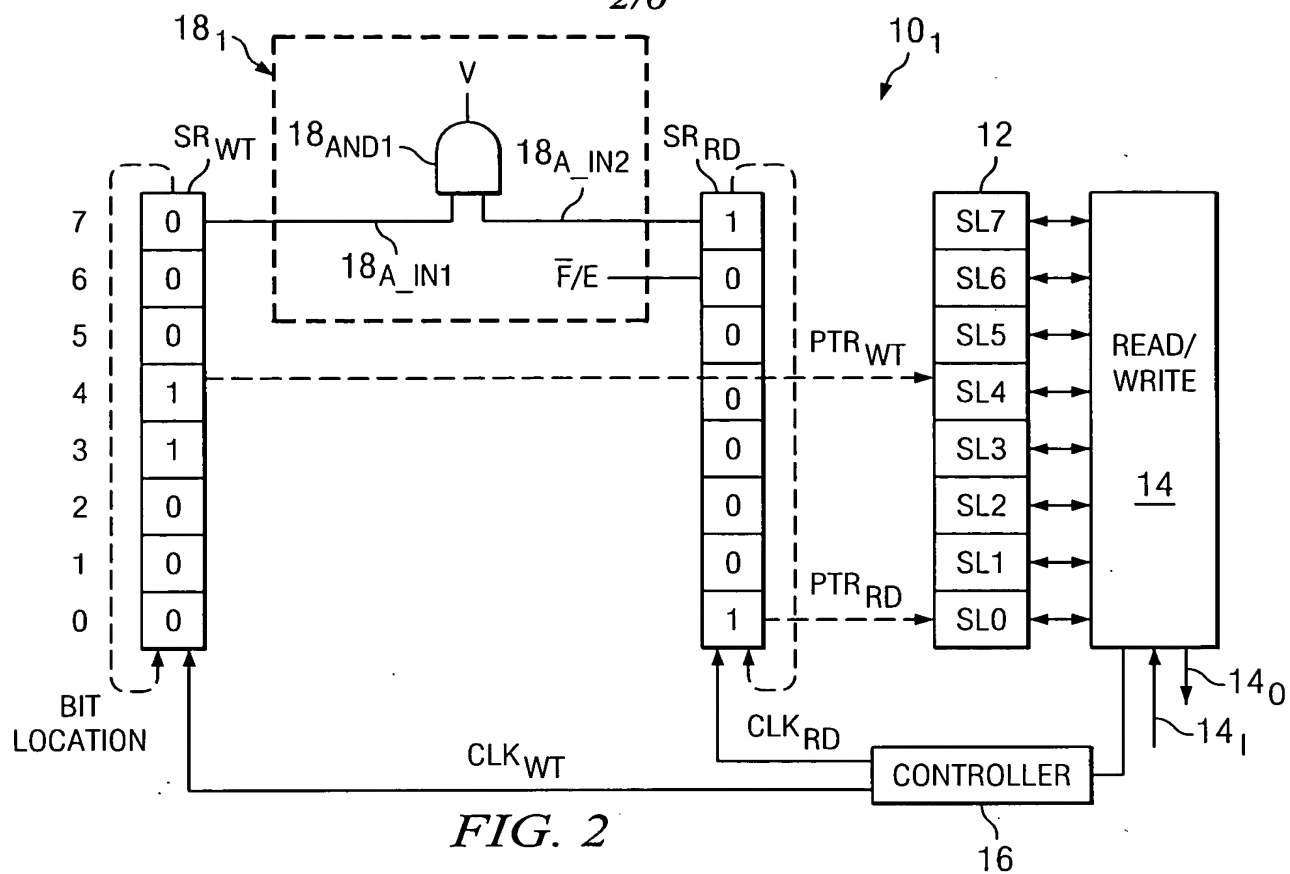


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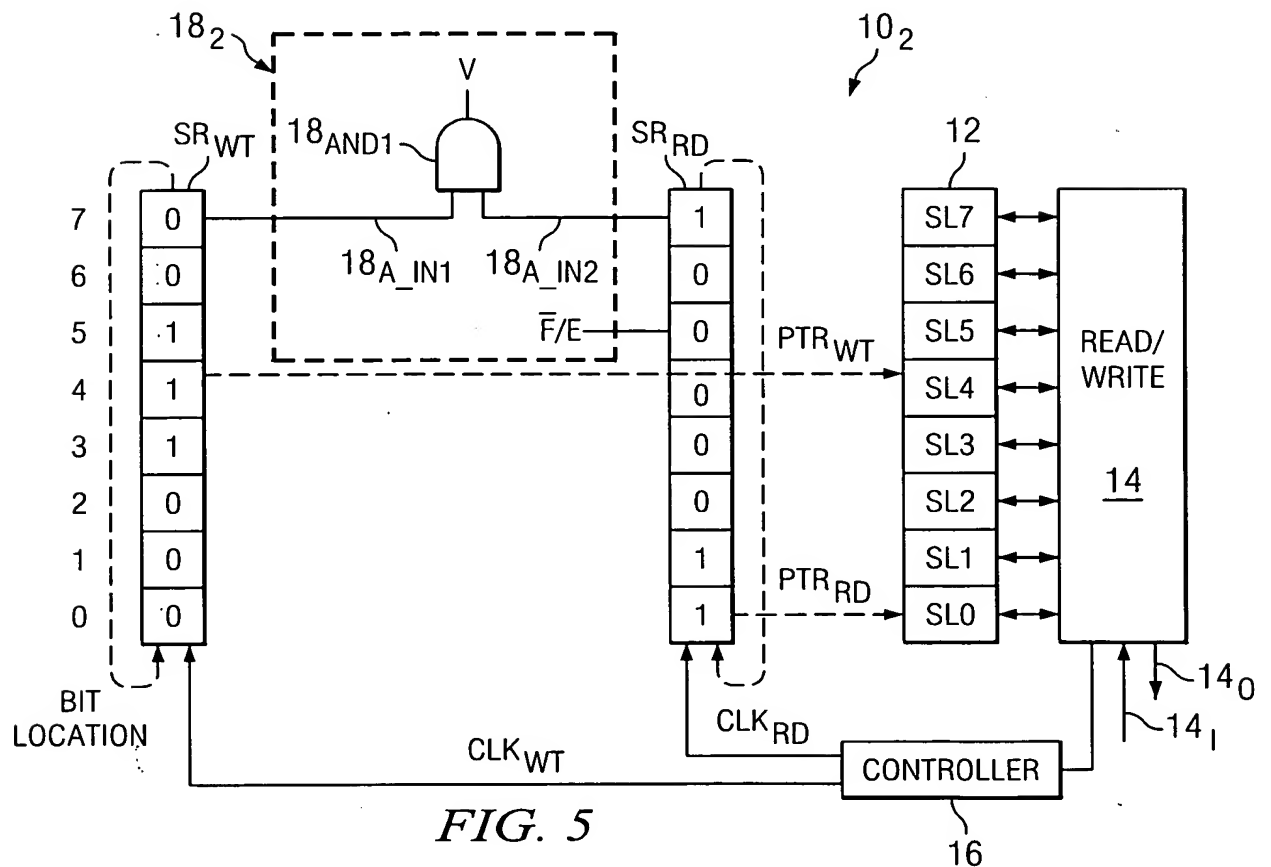
BIT LOCATION	7	6	5	4	3	2	1	0	SEQUENCE
	1	0	0	0	0	0	0	1	$SR_{WT}$
	0	0	0	0	0	0	1	1	$SR_{RD\_1}$
	0	0	0	0	0	1	1	0	$SR_{RD\_2}$
	0	0	0	0	1	1	0	0	$SR_{RD\_3}$
	0	0	0	1	1	0	0	0	$SR_{RD\_4}$
	0	0	1	1	0	0	0	0	$SR_{RD\_5}$
	0	1	1	0	0	0	0	0	$SR_{RD\_6}$
	1	1	0	0	0	0	0	0	$SR_{RD\_7}$

*FIG. 3*

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BIT LOCATION	7	6	5	4	3	2	1	0	SEQUENCE
	1	0	0	0	0	0	0	1	$SR_{RD}$
	0	0	0	0	0	0	1	1	$SR_{WT\_1}$
	0	0	0	0	0	1	1	0	$SR_{WT\_2}$
	0	0	0	0	1	1	0	0	$SR_{WT\_3}$
	0	0	0	1	1	0	0	0	$SR_{WT\_4}$
	0	0	1	1	0	0	0	0	$SR_{WT\_5}$
	0	1	1	0	0	0	0	0	$SR_{WT\_6}$
	1	1	0	0	0	0	0	0	$SR_{WT\_7}$

*FIG. 4*



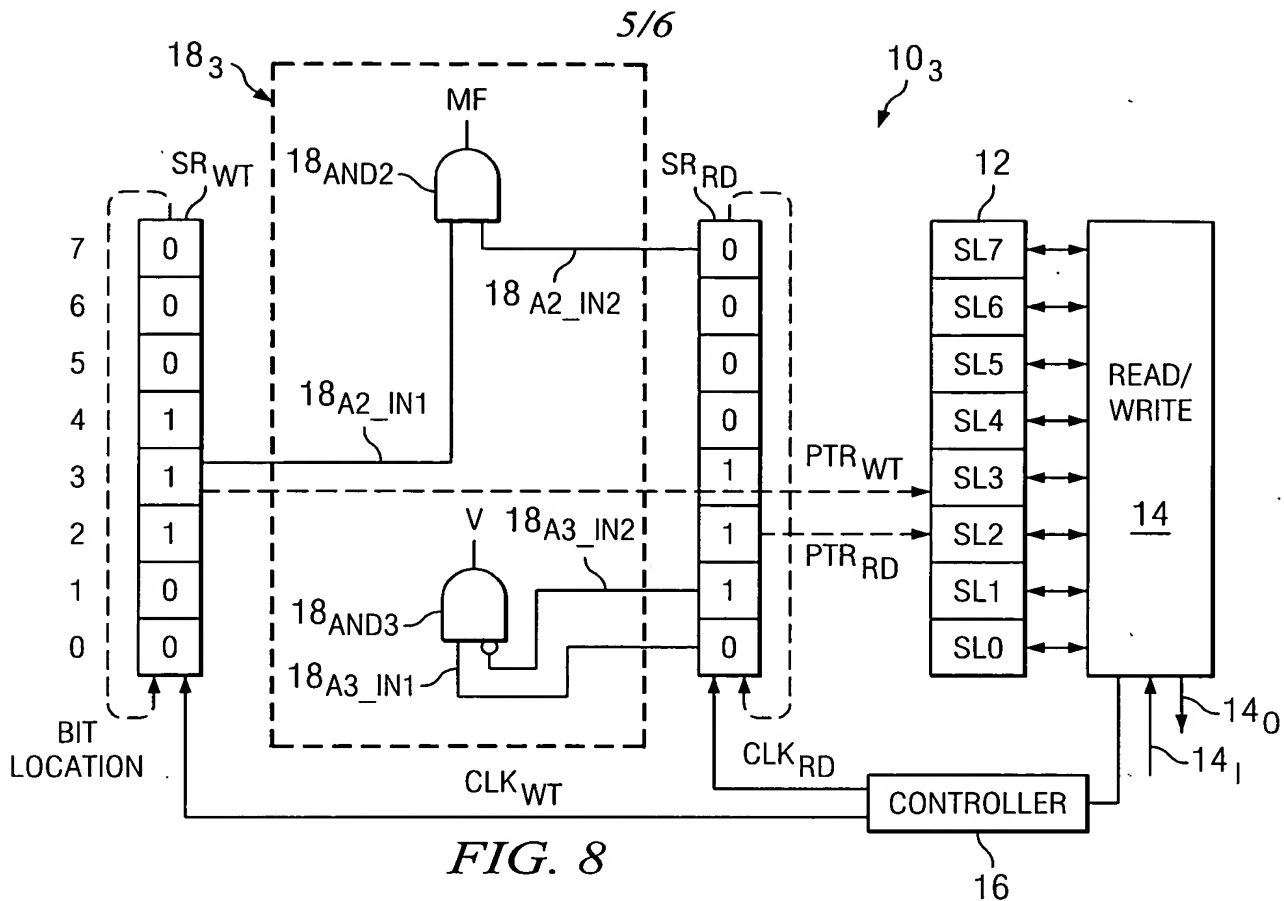
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BIT LOCATION	7	6	5	4	3	2	1	0	SEQUENCE
	1	0	0	0	0	0	1	1	SR <sub>WT</sub>
	0	0	0	0	0	1	1	1	SR <sub>RD_1</sub>
	0	0	0	0	1	1	1	0	SR <sub>RD_2</sub>
	0	0	0	1	1	1	0	0	SR <sub>RD_3</sub>
	0	0	1	1	1	0	0	0	SR <sub>RD_4</sub>
	0	1	1	1	1	0	0	0	SR <sub>RD_5</sub>
	1	1	1	0	0	0	0	0	SR <sub>RD_6</sub>

FIG. 6

BIT LOCATION	7	6	5	4	3	2	1	0	SEQUENCE
	1	0	0	0	0	0	1	1	SR <sub>RD</sub>
	0	0	0	0	0	1	1	1	SR <sub>WT_1</sub>
	0	0	0	0	1	1	1	0	SR <sub>WT_2</sub>
	0	0	0	1	1	1	0	0	SR <sub>WT_3</sub>
	0	0	1	1	1	0	0	0	SR <sub>WT_4</sub>
	0	1	1	1	0	0	0	0	SR <sub>WT_5</sub>
	1	1	1	0	0	0	0	0	SR <sub>WT_6</sub>

FIG. 7



BIT LOCATION	7	6	5	4	3	2	1	0	SEQUENCE
	0	0	0	1	1	1	0	0	SR <sub>WT</sub>
	0	0	0	0	1	1	1	0	SR <sub>RD_1</sub>
	0	0	0	1	1	1	0	0	SR <sub>RD_2</sub>
	0	0	1	1	1	0	0	0	SR <sub>RD_3</sub>
	0	1	1	1	0	0	0	0	SR <sub>RD_4</sub>
	1	1	1	0	0	0	0	0	SR <sub>RD_5</sub>
	1	1	0	0	0	0	0	1	SR <sub>RD_6</sub>
	1	0	0	0	0	0	1	1	SR <sub>RD_7</sub>
	0	0	0	0	0	1	1	1	SR <sub>RD_8</sub>

**FIG. 9**

